Amendments to the Claims:

The following listing of claims will replace any/all prior versions, and listings, of claims in the application, wherein additions are shown in underlined text and deletions are shown in strike-out text or between brackets ([ ]):

1. (Previously Presented) A method of forming an isolation film in a semiconductor device, comprising:

forming a stack structure of a pad oxide film and a photoresist pattern on a semiconductor substrate on which an isolation region is defined, the isolation region having one or more corners and a central portion, the photresist pattern containing silicon;

implementing an over etch so that polymer is formed at the corners of the isolation region to form an etch slant face at one or more corners of the isolation region while etching the semiconductor substrate at the central portion of the isolation region;

forming a trench at the central portion of the isolation region;

oxidizing a surface of the photoresist pattern to form a surface oxide film;

forming an insulating material layer on the entire structure to bury the trench; and

implementing a polishing process until the photoresist pattern has a given thickness and then removing the photoresist pattern and the pad oxide film.

2. (Original) The method as claimed in claim 1, wherein the amount of silicon contained in the photoresist pattern is in the range of from about 7 to about 50%.

3. (Original) The method as claimed in claim 1, wherein the over etch process uses a CHF_3 gas, a CF_4 gas or a mixture thereof as an etch gas to etch the central portion of the isolation region in depth an amount ranging from about 50 to about 400 Å.

4. (Original) The method as claimed in claim 3, wherein a supply flow of CHF_3 is from about 50 to about 70 sccm, the supply flow of CF_4 is from about 30 to about 50 sccm and an Ar gas flow of from about 1000 to about 2000 sccm is supplied as a carrier gas.

5. (Original) The method as claimed in claim 1, wherein the over etch process is implemented for a time period from about 5 to about 30 seconds with a pressure of from about 500 to about 2500 mTorr and a power of from about 600 to about 2000 W is applied.

6. (Original) The method as claimed in claim 1, wherein a width of the etch slant face is from about 0.02 μm to about 0.07 μm and a tilt angle of the sidewall of the etch slant face is from about 20 to about 50°.

7. (Original) The method as claimed in claim 1, wherein the surface oxide film is formed by means of an O_2 plasma processing.

8. (Original) The method as claimed in claim 7, wherein the O_2 plasma processing is implemented at a temperature ranging from about 50 to about 200 °C by means of an O_2 ashing process or an O_2 ion implantation process.

9. (Original) The method as claimed in claim 1, wherein the insulating material layer is formed using a low thermal oxide film at a temperature ranging from about 50 to about 300 °C.

10. (Currently Amended) A method of forming an isolation film in a semiconductor device, comprising the steps of:

forming a stack structure of a pad oxide film, an amorphous silicon layer, an anti-reflection film and a photoresist pattern on a semiconductor substrate on which an isolation region and an active region are ~~is~~ defined;

implementing an over etch so that polymer is formed at a corner of the isolation region to form an etch slant face at the corner of the isolation region while etching the semiconductor substrate at the central portion of the isolation region;

forming a trench at the central portion of the isolation region;

removing the photoresist pattern and the anti-reflection film;

oxidizing the surface of the amorphous silicon layer to form a surface oxide film;

forming an insulating material layer on the entire structure to bury a the trench; and

implementing a polishing process until the insulating material layer is at a given thickness and then removing the amorphous silicon layer and the pad oxide film, thereby forming an isolation film, wherein ~~the width of~~ the top surface of the isolation film ~~is widened up to an~~ protrudes higher than the active region ~~in~~ of the semiconductor substrate.

11. (Currently Amended) The method as claimed in claim 10, wherein the over etch process uses a CHF_3 gas, a CF_4 gas or a mixed gas of them as an etch gas to etch ~~a central portion of the isolation region in depth in an amount ranging from~~ to a depth of about 50 Å to about 400 Å.

12. (Currently Amended) The method as claimed in claim 10, wherein the width of the etch slant face ranges from about 0.02μm to about 0.07μm, and [a] the tilt angle ~~of the sidewall~~ of the etch slant face ranges from about from 20° to about 50°.

13. (Currently Amended) The method as claimed in claim 10, further comprising the step of ~~before the surface of the amorphous silicon layer is oxidized after the anti-reflection film is removed,~~ oxidizing the sidewall and bottom of the trench to form a surface oxide film at the sidewall and bottom of the trench before the surface of the amorphous silicon layer is oxidized and after the anti-reflection film is removed.

14. (Currently Amended) The method as claimed in claim 10, wherein the surface oxide film is formed by means of an O_2 plasma process[ing].

15. (Currently Amended) The method as claimed in claim 14, wherein the O_2 plasma process[ing] is implemented at a temperature ranging from about 50 °C to about 200 °C by means of an O_2 ashing process or an O_2 ion implantation process.

16. (Currently Amended) A method of forming an isolation film in a semiconductor device, comprising the steps of:

stacking a pad oxide film, an amorphous silicon layer, a hard mask film, ~~an anti-reflection film~~ and a photoresist pattern on a semiconductor substrate on which an isolation region and an active region are ~~is~~ defined;

implementing an over etch so that polymer is formed at a corner of the isolation region to form an etch slant face at the corner of the isolation region while etching the semiconductor substrate at the central portion of the isolation region;

etching a part of the semiconductor substrate using the polymer ~~film~~ as an etch mask to form a trench at the central portion of the isolation region;

burying the trench with an insulating film and then removing the polymer ~~film~~ and the hard mask film;

implementing an O_2 plasma oxidization process to oxidize the top and sidewall of the amorphous silicon ~~film~~ layer, thus forming an oxide film on the top and sidewall of the amorphous silicon ~~film~~ layer;

etching the oxide film on the top of the amorphous silicon ~~film~~ layer; and

etching the amorphous silicon ~~film~~ layer and the pad oxide film below the oxide film on the side of the amorphous silicon ~~film~~ layer, thereby forming an isolation film, wherein ~~the width of~~ the top surface of the isolation film ~~is widened up to an~~ protrudes higher than the active region ~~in~~ of the semiconductor substrate.

17. (Currently Amended) The method as claimed in claim 16, wherein the O_2 plasma oxidization process ~~is~~ implemented to oxidize a the top and sidewall of the amorphous silicon ~~film~~ layer ~~using~~ uses a plasma ashing method and an O_2 ion implantation method having a temperature ranging from about 50 °C to about 200 °C.

18. (Currently Amended) The method as claimed in claim 16, wherein the polymer ~~film~~ is formed by etching about 200Å of the semiconductor substrate using a gas such as CF_4 and CHF_3.